Evaluation of the Reliability of Electro-Photonic Accelerators

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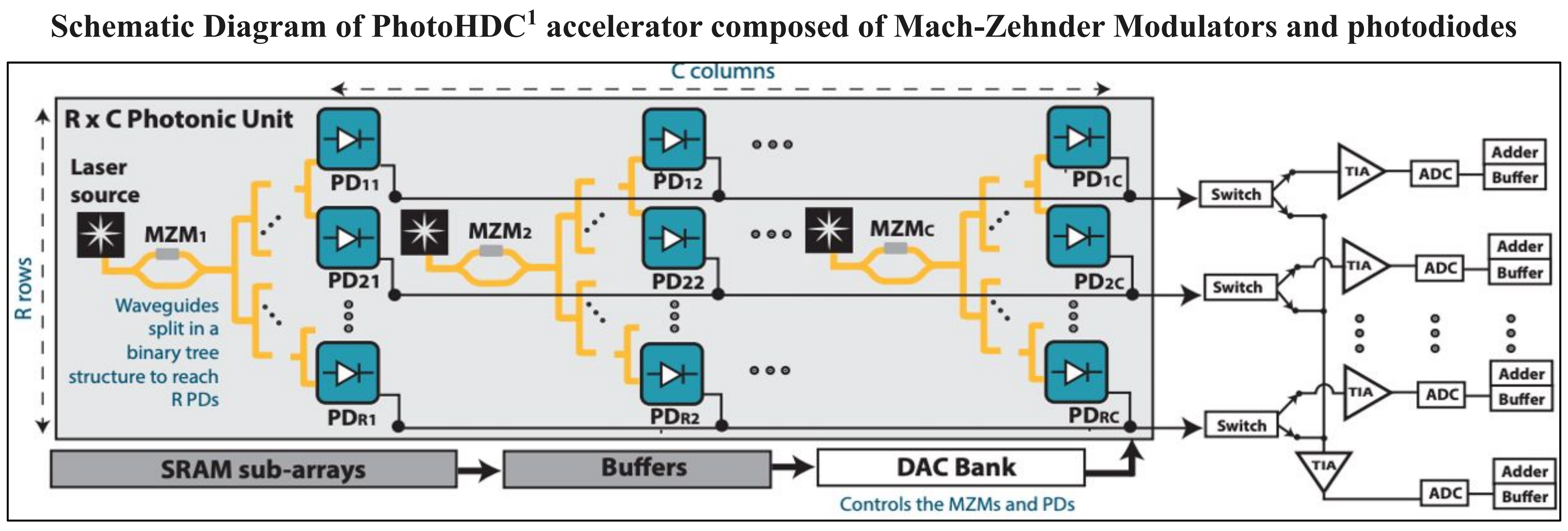
1. Introduction

- Photonic computing uses light to represent and process data rather than electricity
- With photonics, we can manipulate light to perform fast and energy efficient Matrix-Vector Multiplications (MVMs)
- Since the majority of operations in Machine Learning (ML) models are MVMs, accelerating their computation significantly enhances the speed and performance of ML applications
- Given the complexity of photonic architectures, simulation tools capable of predicting their response are crucial in the performance evaluation and optimization before manufacturing

Schematic Diagram of PhotoHDC[1] accelerator composed of Mach-Zehnder Modulators and photodiodes



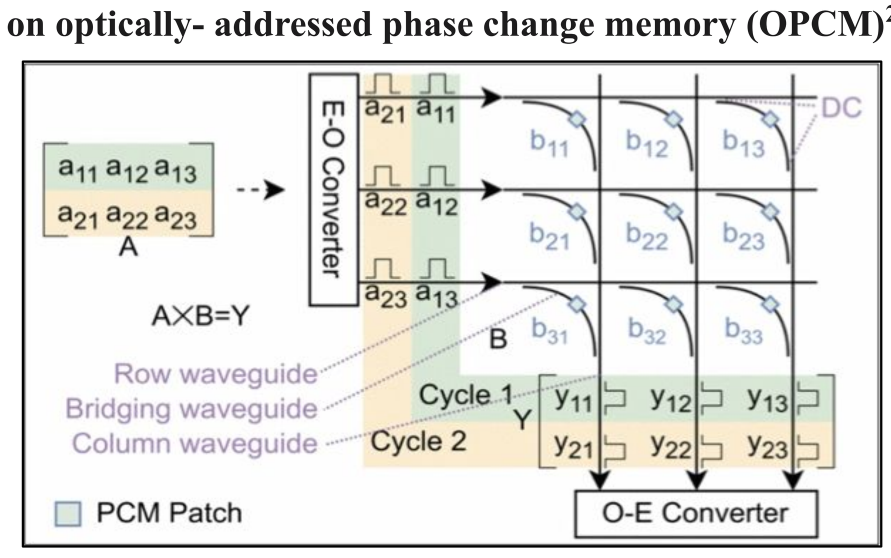
PhotoHDC

- First-ever electro-photonic accelerator for Hyper Dimensional Computing (HDC)
- Lightweight, efficient, and fast

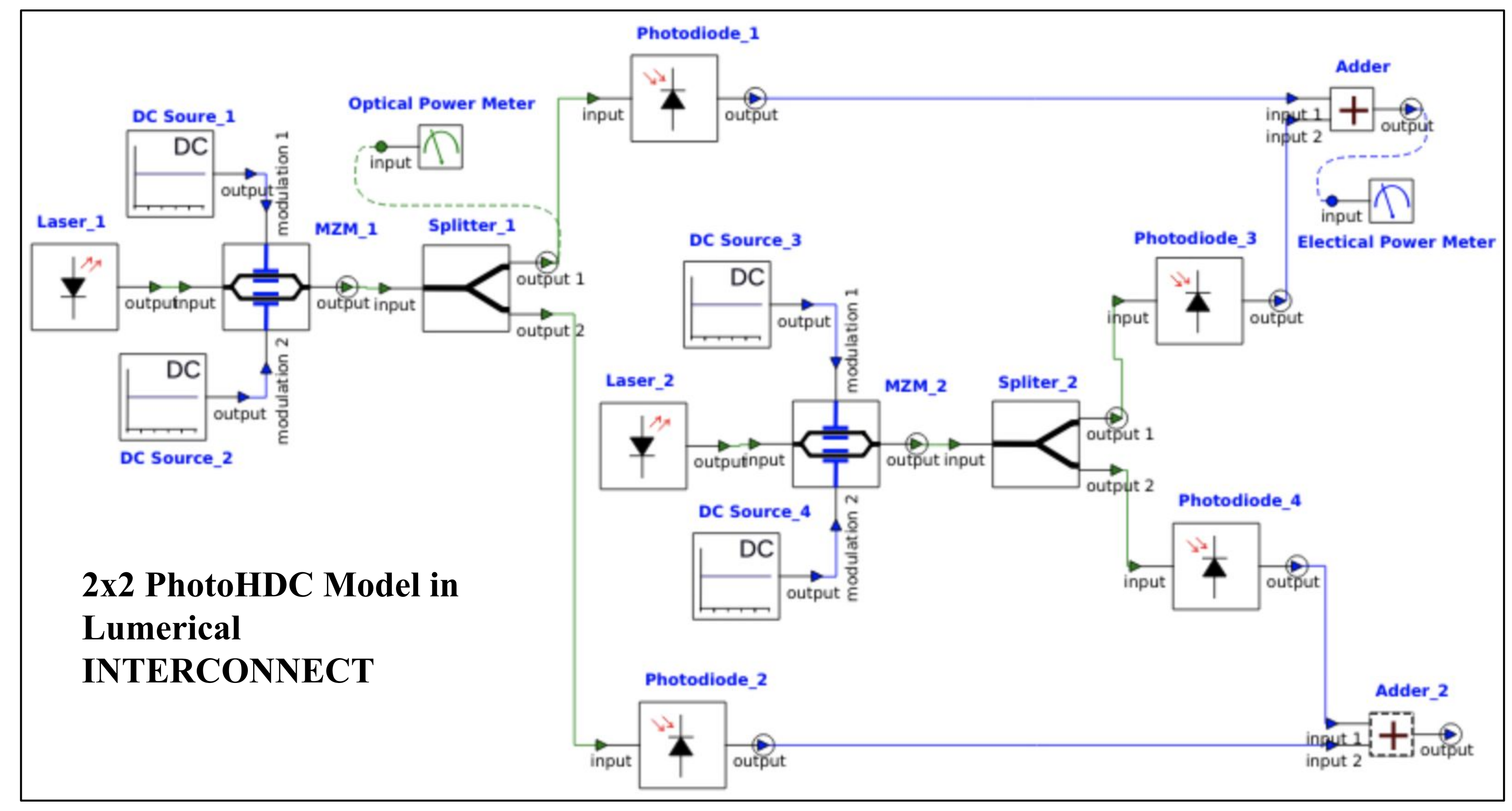
PiM OPCM Crossbar Array

- Aims to reduce the costly data transfers between memory and computing hardware by using optical signals
- Tends to be more energy efficient due to its use of optical signals

Processing-in-Memory (PiM) computing architecture based on optically- addressed phase change memory (OPCM)[2]

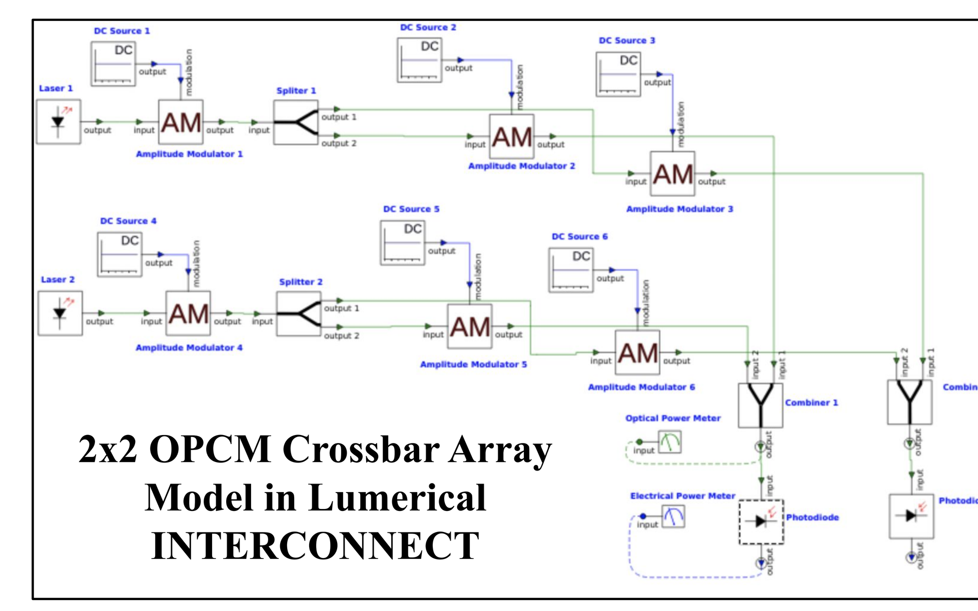


2. Methods



2x2 PhotoHDC Model in Lumerical INTERCONNECT

1. Modelled both architectures in Lumerical INTERCONNECT
2. Created a script able to model either architecture in any inputted size
3. Performed a Monte Carlo Analysis on the following architecture sizes: 16×16, 32×32, 64×64, 128×128
4. For each architecture size, I performed a Monte Carlo Analysis with variation levels of 1%, 2%, 5%, and 10% for 1,000 runs
5. The optical power was measured at the end of the optical path

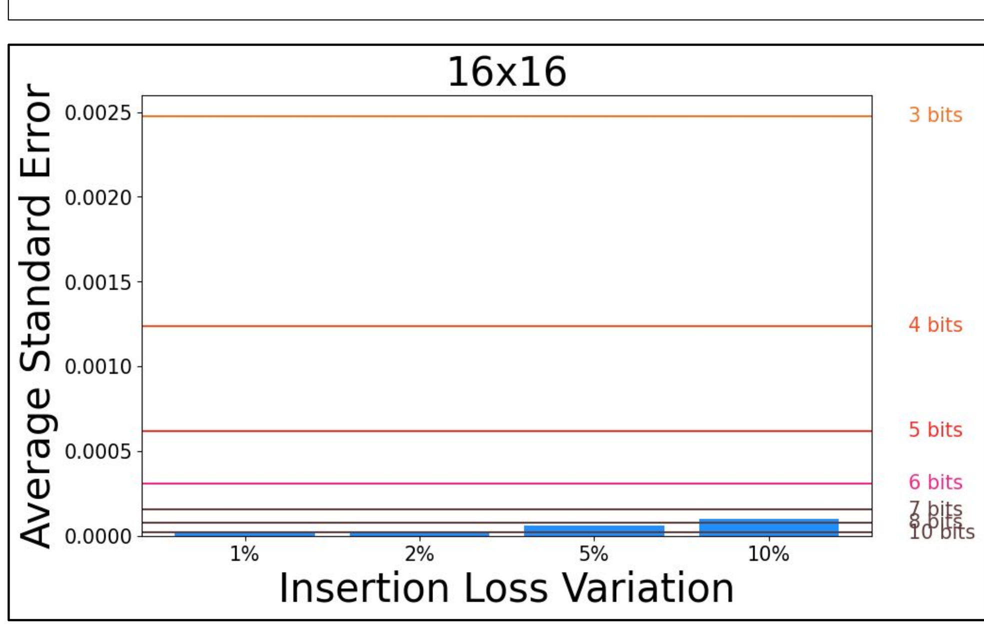


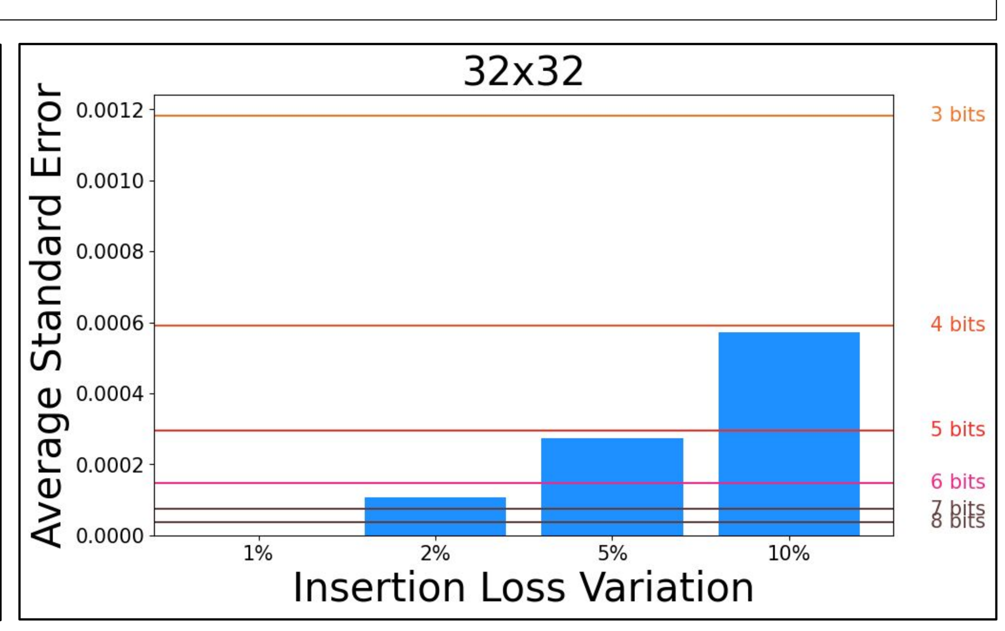
2x2 OPCM Crossbar Array Model in Lumerical INTERCONNECT

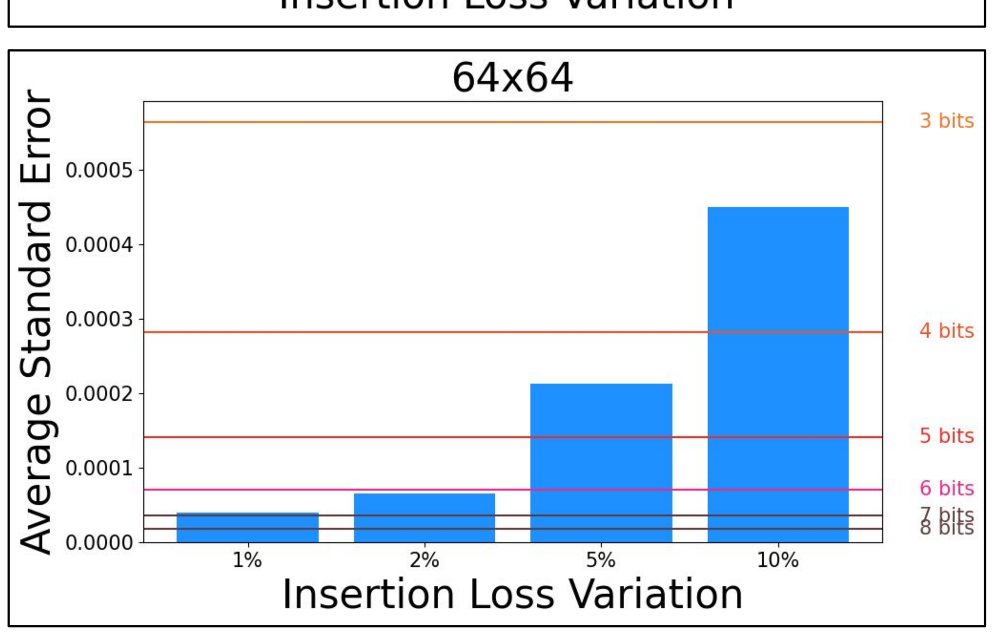
3. Results

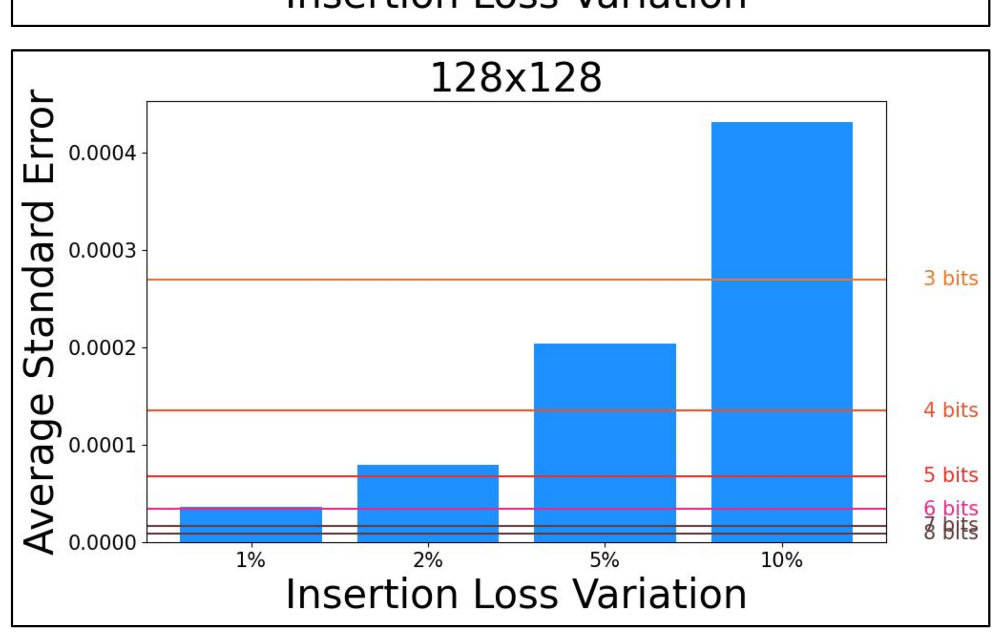
Here, we analyze the error tolerance of PhotoHDC to estimate the achievable bit precision:

- Blue bars represent the average standard error of each insertion loss (IL) variation level
- Vertical lines indicate the bit precision that a given PhotoHDC architecture size and variation combination can achieve









Observations:

- The lower the IL variation, the smaller the average standard error is across all array sizes
- Larger architectures achieve lower bit precisions
- Bit precisions attainable by each array size with 2% variation:
  - 128×128 can achieve 4-bit precision
  - 64×64 can achieve 6-bit precision
  - 32×32 can achieves 6-bit precision
  - 16×16 can achieves 8-bit precision

Overall, as we increase the array size, the loss increases and the bit precision we can achieve becomes lower

4. Discussion/Conclusions

Summary:

- Photonic circuits can be precisely modeled using S-matrix-based simulations
- The Monte Carlo Analysis simulation allowed us to analyze the error tolerance of PhotoHDC
- We found that with an increased PhotoHDC array size, there is a decreased bit precision
- Furthermore, with practical levels of variance, the 128×128 PhotoHDC array architecture achieved 4-bit precision, which agrees with the precision level used in preliminary work [1] from our group

Future Works

- Additional losses and variations on all the elements' parameters will be implemented to increase model accuracy
  - Waveguide lengths and losses between each element were not considered, however they are small compared to other losses, so the difference is almost negligible
- We will extend the Monte Carlo Analysis to the OPCM crossbar array architecture
- A comparison will be done between the performance of PhotoHDC and the OPCM crossbar array architectures in order to find the most practical option
- A simulation using input values from an ML model will be executed on both architectures to test their accuracies

References

[1] Fayza, F.; Demirkiran, C.; Chen, H.; Liu, C.-K.; Mohan, A.; Errahmouni, H.; Yun, S.; Imani, M.; Zhang, D.; Bunandar, D.; Joshi, A. Towards Efficient Hyperdimensional Computing Using Photonics. https://arxiv.org/pdf/2311.17801

[2] Yang, G.; Demirkiran, C.; Kizilates, Z. E.; Ocampo, C. A.; Coskun, A. K.; Joshi, A. Processing-in-Memory Using Optically-Addressed Phase Change Memory. 2023 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED) 2023. DOI:10.1109/islped58423.2023.10244409.

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